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Terms: [patno=6054872](#) ([Edit Search](#))

997035 (08) 6054872 April 25, 2000

UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT  
**6054872**

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April 25, 2000

Semiconductor integrated circuit with mixed gate array and standard cell

**REISSUE:** Reissue Application filed Sep. 27, 2001 (O.G. Jan. 29, 2002) Ex. Gp.: 2819; Re. S.N. 09/963,735, (O.G. January 29, 2002)

**INVENTOR:** Fudanuki, Nobuo, Tokyo, JP; Sei, Toshikazu, Tokyo, JP

**APPL-NO:** 997035 (08)

**FILED-DATE:** December 23, 1997

**GRANTED-DATE:** April 25, 2000

**PRIORITY:** December 27, 1996 - 8-351360, Japan (JP); December 12, 1997 - 9-343278, Japan (JP)

**ASSIGNEE-AT-ISSUE:** Kabushiki Kaisha Toshiba, Kawasaki, JP

**ASSIGNEE-AFTER-ISSUE:** May 19, 1998 - ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS)., KABUSHIKI KAISHA TOSHIBA 72 HORIKAWA- CHO, SAIWAI-KU, KAWASAKI-SHI KANAGAWA-KE N JAPAN, Reel and Frame Number: 009182/0483

**LEGAL-REP:** Foley & Lardner

**PUB-TYPE:** April 25, 2000 - Utility Patent having no previously published pre-grant publication (A)

**PUB-COUNTRY:** United States (US)

**US-MAIN-CL:** 326#39

**US-ADDL-CL:** 326#101

**CL:** 326

**SEARCH-FLD:** 326#39, 326#41, 326#101.-103, 327#403.-405, 327#565, 327#566

**IPC-MAIN-CL:** H 03K019#177

**PRIM-EXMR:** Tokar, Michael

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7/07/03

US 6,054,872

09/963735

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Selected file: PLUSPAT

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Query/Command : us6054872/pn

\*\* SS 1: Results 1

Search statement 2

Query/Command : prt fu legalall max

1 / 1 PLUSPAT - @QUESTEL-ORBIT  
PN - US6054872 A 20000425 [US6054872]  
TI - (A) Semiconductor integrated circuit with mixed gate array and standard cell  
PA - (A) TOKYO SHIBAURA ELECTRIC CO (JP)  
PA0 - Kabushiki Kaisha Toshiba, Kawasaki [JP]  
IN - (A) SEI TOSHIKAZU (JP); FUDANUKI NOBUO (JP)  
AP - US99703597 19971223 [1997US-0997035]  
PR - JP35136096 19961227 [1996JP-0351360]  
JP34327897 19971212 [1997JP-0343278]  
IC - (A) H03K-019/177  
EC - H03K-019/173C1  
PCL - ORIGINAL (O) : 326039000; CROSS-REFERENCE (X) : 326101000  
DT - Basic  
CT - US4207556; US4750027; US4809029; US4811073; US4949275; US4967100; US4969029; US5051917; US5155390  
STG - (A) United States patent  
AB - The present invention relates to a semicustom ASIC, in which a plurality of standard cell rows are arranged. The standard cell and basic cells used in a gate array are mixedly mounted on the same chip. Respective cell rows are composed of a plurality of standard cells with an empty space. The basic cells used in the gate array are arranged as dummy cells. They are disposed in wiring channel regions between the plurality of standard cells or empty spaces between the standard cells in a same standard cell row. Only the latter may be used if the channelless type standard cells are employed. A changing request can be satisfied by forming metal wiring layers on the gate array basic cells when there is a necessity of changing circuit design or pattern. Since the circuit can be modified without change of gate polysilicon regions and source/drain regions underlying the metal wiring layers, design and manufacture can be effected in a short period of time.  
UP - 2000-17

1 / 1 LGST - @LEGSTAT  
PN - US 6054872 [US6054872]  
AP - US 997035/97 19971223 [1997US-0997035]  
DT - US-P

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US 6,054,872

09/963735

**ACT** - 19971223 US/AE-A  
APPLICATION DATA (PATENT)  
US 997035/97 19971223 [1997US-0997035]

20000425 US/A  
PATENT

20020129 US/RF  
REISSUE APPLICATION FILED  
20010927

**UP** - 2002-06

1 / 1 CRXX - ©CLAIMS/RRX  
**AN** - 3313811  
**PN** - 6,054,872 A 20000425 [US6054872]  
**PA** - Toshiba Corp JP  
**PT** - E (Electrical)  
**ACT** - 20010927 REISSUE REQUESTED  
ISSUE DATE OF O.G.: 20020129  
REISSUE REQUEST NUMBER: 09/963735  
EXAMINATION GROUP RESPONSIBLE FOR REISSUEPROCESS: 2819

Reissue Patent Number:

**UP** - 2002-05  
**UACT** - 2002-01-29

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1 Patent Groups  
\*\* SS 2: Results 2

Search statement 3

**Query/Command : famstate nonstop**

1 / 2 PLUSPAT - ©QUESTEL-ORBIT - image  
**PN** - JP10242289 A 19980911 [JP10242289]  
**STG** - (A) Doc. Laid open to publ. Inspec.  
**TI** - (A) INTEGRATED CIRCUIT AFTER STANDARD CELL SYSTEM  
**PA** - (A) TOKYO SHIBAURA ELECTRIC CO  
**PA0** - (A) TOSHIBA CORP  
**IN** - (A) FUDANUKI NOBUO; SEI TOSHIKAZU  
**IC** - (A) H01L-021/82 H01L-027/118  
**AP** - JP34327897 19971212 [1997JP-0343278]  
**PR** - JP34327897 19971212 [1997JP-0343278]  
JP35136096 19961227 [1996JP-0351360]

2 / 2 PLUSPAT - ©QUESTEL-ORBIT  
**PN** - US6054872 A 20000425 [US6054872]  
**STG** - (A) United States patent  
**TI** - (A) Semiconductor integrated circuit with mixed gate array and

7/07/03

US 6,054,872

09/963735

standard cell  
**PA** - (A) TOKYO SHIBAURA ELECTRIC CO (JP)  
**PA0** - Kabushiki Kaisha Toshiba, Kawasaki [JP]  
**IN** - (A) SEI TOSHIKAZU (JP); FUDANUKI NOBUO (JP)  
**IC** - (A) H03K-019/177  
**AP** - US99703597 19971223 [1997US-0997035]  
**PR** - JP35136096 19961227 [1996JP-0351360]  
JP34327897 19971212 [1997JP-0343278]  
**EC** - H03K-019/173C1  
**PCL** - ORIGINAL (O) : 326039000; CROSS-REFERENCE (X) : 326101000  
**DT** - Basic  
**UP** - 2000-17

1 / 1 *LEGALI - ©LEGSTAT*  
**PN** - US 6054872 [US6054872]  
**AP** - US 997035/97 19971223 [1997US-0997035]  
**DT** - US-P  
**ACTE** - 19971223 US/AE-A  
APPLICATION DATA (PATENT)  
US 997035/97 19971223 [1997US-0997035]  
  
20000425 US/A  
PATENT  
  
20020129 US/RF  
REISSUE APPLICATION FILED  
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**UP** - 2002-06

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